AMENDMENTS TO THE CLAIMS:

Please cancel without prejudice claims 2-5, 7, 8 and 11 and amend claims 1, 6, 9-11, 13, 20 and 22 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A switching circuit comprising a bridge circuit, said bridge circuit comprising:

an input operable to receive a direct current, DC, supply ~~signal~~ of nominal voltage $+V_S$ ~~+VS~~,

an output, said output having opposed ends;

first and second bridge arms, said arms having corresponding first and second switches operable in response to first and second switching signals to be switched between on and off states, wherein ~~such that~~ switching between various combinations of on and off states produces an electrical signal at the opposed ends of said output with voltage pulses at levels of nominally $+V_S$, 0V, and $-V_S$, ~~+VS, 0V and -VS~~ and

a voltage sensor for producing a signal indicative of a voltage indicative of the DC Supply ~~offset in the switching circuit~~.

2. (cancelled).

3. (cancelled).

4. (cancelled).

5. (cancelled).

6. (currently amended) A switching circuit according to claim ~~5~~1, ~~wherein the voltage~~further comprising a current sensor for producing a signal indicative of~~is arranged to measure~~ the current flowing through the output.

7. (cancelled).

8. (cancelled).

9. (currently amended) A switching circuit according to claim ~~8~~1, wherein the bridge circuit is a half-bridge with the third and fourth arms having diodes.

10. (currently amended) A switching circuit according to claim ~~8~~1, wherein the first and second switches are transistors.

11. (currently amended) A switching circuit according to claim ~~8~~1, wherein an electromagnet is connected across the output of the bridge circuit.

12. (cancelled).

13. (currently amended) A method of operating a switching circuit comprising an input that receives a DC ~~signal~~supply of nominal voltage ~~+VS~~+V_S, an output and first and second switches, the method comprising the steps of:

(a) receiving a voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the output in a period;

(b) generating first and second switching signals with reference to the voltage demand signal and with reference to a voltage offset in the switching circuit; and

(c) applying the first and second switching signals to the first and second switches respectively during the period;

wherein the switching signals cause the switches to switch between on and off states, switching between various combinations of on and off states of the first and second switches

producing an electrical signal at the output with voltage pulses at levels of nominally ~~+VS, 0V and -VS~~ $+V_S$, 0V and $-V_S$, the first and second switching signals being generated such that an average voltage of the electrical signal supplied to the output during the period is substantially equal to the desired voltage.

14. (currently amended) The method of claim 13, wherein at least one of the first and second switching signals is generated with reference to a voltage signal indicative of the DC ~~signal~~supply such that the at least one first or second switching signal compensates for fluctuations in the DC supply.

15. (original) The method of claim 14, wherein the voltage signal is passed through a filter to obtain a predictive measure of fluctuations in the DC supply.

16. (original) The method of claim 15, wherein the voltage signal is passed through a finite impulse response filter.

17. (previously presented) The method of claim 13, wherein at least one of the first and second switching signals is generated to compensate for a voltage drop across a diode and/or transistor in the switching circuit.

18. (original) The method of claim 17, wherein the at least one first or second switching signal is generated with reference to a current signal indicative of the current flowing through the output and a representative resistance of the diode or transistor.

19. (currently amended) The method of claim 13, wherein at least one of the first or second switching signals is generated with reference to a measure of a voltage offset caused by a slow response ~~times~~ in generating the first or second switching signals.

20. (currently amended) The method of claim 13, wherein the switching circuit comprises a bridge circuit having an input that receives ~~a~~the DC supply~~signal of voltage +VS~~, an

output and first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the output.

21. (original) The method of claim 20, wherein the bridge circuit is a half-bridge with the third and fourth arms having diodes.

22. (currently amended) The method of claim 20, wherein the first and second switches are transistors and the method comprises the step of switching the transistors between on and off states corresponding to substantially ~~maximum~~minimum voltage drop and substantially minimum current flow, respectively, through the transistors.

23. (previously presented) The method of claim 13 comprising the step of generating pulsed first and second switching signals.

24. (original) The method of claim 23 comprising the step of generating the first and second switching signals according to a rule that the first and second switches are not switched concurrently.

25. (previously presented) The method of claim 23 comprising the step of generating the first and second switching signals according to a rule that the signals are to have no more than one pulse per period.

26. (original) The method of claim 25 comprising the step of generating the first and second switching signals according to a rule that any pulse should be positioned symmetrically about the centre of the period.

27. (original) The method of claim 26 comprising the step of generating the first and second switching signals according to the rule that where pulses cannot be centred symmetrically, the longer and shorter sides of the asymmetric pulses are alternated between the leading edge side and the trailing edge side for successive pulses.

28. (previously presented) The method of claim 23 comprising the step of generating the first and second switching signals according to a pulse width modulation scheme.

29. (previously presented) The method of claim 23 comprising the step of noise shaping the first and second switching signals.

30. (previously presented) The method of claim 13 comprising the step of receiving a current demand signal indicative of a desired current to be supplied to the output in a period and calculating the voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the output that results in the electrical signal being supplied to the output during the period with a current substantially equal to the desired current.

31. (original) The method of claim 30, wherein the step of calculating the voltage demand signal is performed with reference to a model of the load characteristic of a load connected to the output.

32. (previously presented) The method of claim 30 further comprising the step of generating the voltage demand signal with reference to a current signal indicative of the current flowing through the output.

33. (previously presented) A computer program comprising program code means for performing the method steps of claim 13 when the program is run on a computer and/or other processing means associated with the switching circuit.

34. (previously presented) A computer program product comprising program code means stored on a computer readable medium for performing the method steps of claim 13 when the program is run on a computer and/or other processing means associated with the switching circuit.

35. (canceled)

36. (canceled)

37. (canceled)